POCHIREDDY DHARMAJA

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Objective

As a M.Tech VLSI postgraduate with a strong foundation in digital electronics and CMOS design and hands-on experience in HDL coding with EDA tools. Looking to begin my career in VLSI domain and contribute to the development of efficient and reliable integrated circuits.

EDUCATION

Vellore Institute of Technology (VIT) — 2025 - Present
M.Tech in VLSI Design (GPA: 8.15/10.0) — Vellore, Tamil Nadu

Sree Vidyanikaethan Engineering College — 2020-2024
B.Tech in Electronics and Communication Engineering (CGPA: 8.9 / 10.0) — Tirupathi, Andhra Pradesh

Narayana Junior College — 2018-2020
Higher Secondary Education (GPA: 9.6 / 10.0) — Nellore, Andhra Pradesh

Nagarjuna Model School — 2018
Secondary Education (GPA: 10.0 / 10.0) — Kadapa, Andhra Pradesh

Technical Skills

Concepts : FSM, STA, CMOS, Digital Electronics
Languages : Verilog, System Verilog (Basics)
EDA Tools : Cadence Virtuoso, Modelsim, Intel Quartus Prime ,Synopsys VCS
Scripting Languages : Basics on TCL

Projects

RISC-V RV32IM SoC Design (Group Project)

- Developed a 32-bit RISC-V processor using a 2-stage multi-cycle FSM architecture.
- Implemented datapath, control logic and supported arithmetic, mul/div, load/store and branch instructions.
- Interfaced the core with memory and GPIO using AXI bus.

Hybrid 10T Low Power Full Adder -CMOS VLSI Design

- Designed a transistor-level 1-bit hybrid full adder using GDI multiplexer logic in 45-nm CMOS and implemented levelrestoration for full-swing outputs and voltage degradation.
- Simulated in Mentor Graphics (SPICE) and analyzed delay, power and PDP across supply voltages and process corners.
- Achieved ~65% transistor reduction and ~80% improvement in power-delay product compared to conventional CMOS adders.

Asynchronous FIFO Design and Verification

- Designed an asynchronous FIFO with independent read and write clock domains.
- Implemented Gray-coded read/write pointers and double flip-flop synchronizers for safer clock domain crossing.
- Verified full and empty conditions using Verilog testbenches.

Achievements

- GATE Qualified (2025) - AIR 6103.